ABSTRACT

A single transistor random access memory cell has an MOS well, a transfer gate of the transistor and a storage capacitor having a storage node in the well that becomes an inversion layer at a threshold voltage near zero. The inversion layer diffuses to an inversion region beneath the transfer gate when the transfer gate is turned on. For high speed operation, a doped region beneath the transfer gate becomes an inversion layer at a threshold voltage near zero. In this invention, a storage node junction is removed, which removes junction leakage and reduces subthreshold leakage current significantly.